DMAPIN PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - apps www.analog.com/MicroConverter

4 ;

5 ; Date : October 2003

6 ;

7 ; File : DMApin.asm

8 ;

9 ; Description : performs hardware pin driven DMA conversions on a

10 ; single ADC channel.

11 ; Debugger or emulator must be used to view results.

12 ;

13 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

14

15 $MOD842 ; use 8052&ADuC842 predefined symbols

16

0040 17 DMACOUNT EQU 64 ; number of ADC readings to take

0010 18 DMAINIT EQU 10h ; top nibble of DMAINIT = ADC channel

19

20 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

21 ; DEFINE VARIABLES IN INTERNAL RAM

---- 22 DSEG

0060 23 ORG 0060h

0060 24 DMASTOPH: DS 1 ; DMA stop address hi byte

0061 25 DMASTOPL: DS 1 ; DMA stop address lo byte

26

27 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

28 ; DEFINE SEGMENT OF EXTERNAL RAM

---- 29 XSEG

0000 30 ORG 000000h

0000 31 DMASTART: DS DMACOUNT\*2 ; location for DMA results

0080 32 DMASTOP: DS 4 ; location for DMA stop sequence

33

34 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

35 ; BEGINNING OF CODE

---- 36 CSEG

0000 37 ORG 0000h

0000 02004B 38 JMP MAIN ; jump to main program

39

40 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

41 ; INTERRUPT VECTOR SPACE

0033 42 ORG 0033h ; (ADC ISR)

0033 53EFFE 43 ANL ADCCON1,#0FEh ; disable hardware CONVST pin

0036 C3 44 CLR C ; clear C to indicate DMA done

0037 32 45 RETI

46

47 ;====================================================================

48 ; MAIN PROGRAM

004B 49 ORG 004Bh

004B 50 MAIN:

51

52 ; PRECONFIGURE external RAM for DMA capture on a single channel...

004B 75EF00 53 MOV ADCCON1,#00h

004E 900080 54 MOV DPTR,#DMASTOP ; store DMASTOP 16bit value..

0051 858261 55 MOV DMASTOPL,DPL ; ..as a high byte & low byte

0054 858360 56 MOV DMASTOPH,DPH ; (for use in GETSTOPFLAG subr)

0057 900000 57 MOV DPTR,#DMASTART ; set DPTR to DMASTART address

005A 7410 58 SETUP: MOV A,#DMAINIT ; set up x-mem with init value

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005C F0 59 MOVX @DPTR,A

005D A3 60 INC DPTR

005E E4 61 CLR A ; clear second byte

005F F0 62 MOVX @DPTR,A

0060 A3 63 INC DPTR

0061 12008C 64 CALL GETSTOPFLAG ; C cleared if DPTR>=DMAEND

0064 40F4 65 JC SETUP

66

0066 7410 67 MOV A,#DMAINIT ; "dummy" DMA location..

0068 F0 68 MOVX @DPTR,A ; ..to preceed stop command

0069 A3 69 INC DPTR

006A E4 70 CLR A

006B F0 71 MOVX @DPTR,A

006C A3 72 INC DPTR

73

006D 74F0 74 MOV A,#0F0h ; DMA stop command

006F F0 75 MOVX @DPTR,A

76

77 ; CONFIGURE ADC for DMA conversion...

78

0070 75D200 79 MOV DMAL,#0 ; start address for DMA operation

0073 75D300 80 MOV DMAH,#0 ; (must write DMA registers in this

0076 75D400 81 MOV DMAP,#0 ; order: DMAL, DMAH, DMAP)

82

0079 75D840 83 MOV ADCCON2,#040h ; enable DMA mode

007C 75EFAC 84 MOV ADCCON1,#0ACh ; 9.5us conv+acq time

85

007F D2AF 86 SETB EA ; enable interrupts

0081 D2AE 87 SETB EADC ; enable ADC interrupt

88

89 ; LAUNCH DMA conversion... when complete, ADC interrupt will clear C

90

0083 43EF01 91 ORL ADCCON1,#001h ; enable hardware CONVST pin

0086 D3 92 SETB C

0087 40FE 93 JC $ ; wait for DMA to finish

94

0089 00 95 NOP ;.................................... SET BREAKPOINT HERE

96

97 ; REPEAT entire program...

98

008A 80BF 99 JMP MAIN

100

101 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

102 ; SUBROUTINE

103

008C 104 GETSTOPFLAG: ; clears C if DPTR>=DMASTOP

008C D3 105 SETB C

008D E583 106 MOV A,DPH

008F B56005 107 CJNE A,DMASTOPH,RET1 ; C cleared if DPH>=DMASTOPH

0092 E582 108 MOV A,DPL

0094 B56100 109 CJNE A,DMASTOPL,RET1 ; C cleared if DPL>=DMASTOPL

0097 22 110 RET1: RET

111

112 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

113

114 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

DMACOUNT . . . . . . . . . . . . NUMB 0040H

DMAH . . . . . . . . . . . . . . D ADDR 00D3H PREDEFINED

DMAINIT. . . . . . . . . . . . . NUMB 0010H

DMAL . . . . . . . . . . . . . . D ADDR 00D2H PREDEFINED

DMAP . . . . . . . . . . . . . . D ADDR 00D4H PREDEFINED

DMASTART . . . . . . . . . . . . X ADDR 0000H

DMASTOP. . . . . . . . . . . . . X ADDR 0080H

DMASTOPH . . . . . . . . . . . . D ADDR 0060H

DMASTOPL . . . . . . . . . . . . D ADDR 0061H

DPH. . . . . . . . . . . . . . . D ADDR 0083H PREDEFINED

DPL. . . . . . . . . . . . . . . D ADDR 0082H PREDEFINED

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

GETSTOPFLAG. . . . . . . . . . . C ADDR 008CH

MAIN . . . . . . . . . . . . . . C ADDR 004BH

RET1 . . . . . . . . . . . . . . C ADDR 0097H

SETUP. . . . . . . . . . . . . . C ADDR 005AH